REMARKS

This Amendment is in response to the Office Action dated October 20, 2004. Claims 1-18 are pending. Claims 1-18 are rejected. Claims 1, 2, 11, 15, 16, 17 and 18 have been amended for clarification. New claims 19, 20 and 21 have been added. Accordingly, claims 1-21 are now pending in the present application.

Present Invention

A receiver equalizer is disclosed. The receiver equalizer comprises samplers for sampling an incoming input data stream according to plural phases of a sampling clock. Each sampler produces a demultiplexed data sample that changes at a slower rate than the incoming signal. The equalizer includes a plurality of multi-tap finite impulse response (FIR) filters. Each FIR filter, in an analog domain, for each demultiplexed data sample, weights said demultiplexed data sample and at least one previous demultiplexed data sample, and combines said weighted data samples to produce an equalized demultiplexed data value. Each FIR filter includes at least one scaler. Each of the scalers has a dedicated tap weight.

A multi-tap analog finite impulse response filter is disclosed. The FIR filter comprises at least one combined voltage-current converter and scaler that produces a first current from an input voltage which is proportional to a product of a previous data sample voltage and a weight associated with said previous data sample tap and a voltage-current converter that produces a second current which is proportional to an instance data sample voltage. The FIR filter includes an adder circuit which subtracts the second current from the first current to produce a third current; and a converter circuit which converts the third current to a voltage corresponding to the equalized data voltage.

Claim Rejections – 35 USC 103

The Examiner states,

2. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (5,907,295) in view of Khoury (US 5,931,898).

Lin discloses an up sampling converter (Fig. 5A) comprising the claimed limitations:

In claims 1, 9, 11-13, 15, "a receiver equalizer, comprising samplers for sampling an incoming input data stream according to plural phases of a sampling clock, each sampler producing a data sample" (30), "a multi-tap finite impulse response (FIR) filter for each data sample, weights said data sample and at least one previous data sample, and combines said weighted data samples to produce an equalized data bit" (44).

Lin fails to teach that the operations performed by the claimed FIR are in analog domain.

Khoury discloses a FIR wherein the operation of "weighting" and "combining" are done in analog domain (see Fig. 2). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Lin's circuit using Khoury's teachings to have the weighting and combining operations performed using analog circuits. Such modification is necessary when the specification of a particular system calls for analog components.

With respect to claims 2, 16-18, Lin and Khoury, taken collectively, disclose all the subject matters claimed, as described above. Khoury (col. 4, line 45-col. 5, line 4) further teaches "a first current source that produces a first current which is proportional to a product" (Fig. 2, element 18), "a second current source that produces a second current which is proportional to an instance data sample" (Fig. 2, INP, 34A), "an adder circuit which subtracts the second current source the first current to produce a third current" (Fig. 1, 19A, 19B). With respect to "a converter circuit which converts the third current to a voltage corresponding to the equalized data bit," it would have been obvious to one of ordinary skill in the art at the time of the invention to employ a current-to-voltage converter, which is widely available in the industry, to convert the equalized data bit from current to voltage in view of Khoury's teachings on col. 8, lines 15-21.

With respect to claims 3-8, Lin and Khoury, taken collectively, disclose all the subject matters claimed, as described above. The limitations regarding the characteristics of the equalizer or communication channel recites the intended use of the claimed invention and do not result in a structural difference between the claimed invention and the prior art.

With respect to claims 10 and 14, Lin and Khoury, taken collectively, disclose all the subject matters claimed, as described above. Lin also teaches "second samplers for sampling and holding the equalized data bit values" (Fig. 5B, 36, 38). The claimed limitation regarding "sense amplifiers for converting the sampled equalized data bit values to digital values" would have been an obvious modification, at the time of the invention, to the system achieved using Lin's and Khoury's teachings described above. Such analog to digital conversion, using well-known sense amplifiers, is needed when digital data is required at the subsequent stage in the design system.

Applicant respectfully traverses this rejection. The key differentiation of the recited invention from Lin and Khoury are described in summary form below.

(1) After the data analog values are sampled, they are processed at a slower rate than

the input data frequency by the FIR filter, thus relaxing the circuit speed requirements significantly to make it suitable for high-speed operation.

(2) Each scale has its own dedicated tap weight, so FIR accuracy is not degraded due to mismatch of the stages, while in Khoury's implementation, the tap weights are rotated from one scaler to another. The latter causes the scaler mismatch to degrade the accuracy of the tap weight scaling.

(3) It performs FIR filtering on the demultiplexed data samples of the input serial stream, and generate demultiplexed equalized data values

(4) The product of input data samples and their associated tap weights are performed in a single open-loop analog stage

The Lin and Khoury references neither singly or in combination disclose or suggest such a cooperation.

Claims 1-15

Independent claims 1, 11 and 15 are reproduced in their entirety hereinbelow.

1. A receiver equalizer, comprising:
samplers for sampling an incoming input data stream according to plural phases of a sampling clock, each sampler producing a demultiplexed data sample that changes at a slower rate than the incoming signal; and
a plurality of multi-tap finite impulse response (FIR) filters, where each FIR filter, in an analog domain, for each demultiplexed data sample, weights said demultiplexed data sample and at least one previous demultiplexed data sample, and combines said weighted data samples to produce an equalized demultiplexed data value, wherein each FIR filter includes at least one scaler, wherein each of the scalers has dedicated tap weight.

11. A method for equalizing an incoming input data stream, comprising:
sampling the input data stream according to plural phases of a sampling clock to produce demultiplexed data samples changing at a slower rate than the incoming signal; and
filtering the slow changing demultiplexed data samples with a plurality of analog multi-tap finite impulse response (FIR) filters, having dedicated tap weights, to produce demultiplexed equalized data values.

15. A receiver equalizer, comprising:

means for sampling the input data stream according to plural phases of a sampling clock to produce demultiplexed data samples changing at a lower rate than the incoming signal; and

means for filtering the slower rate demultiplexed data samples with a plurality of analog multi-tap finite impulse response (FIR) filters to produce demultiplexed equalized data values;

means for sampling and holding the demultiplexed equalized data values; and

means for converting the sampled equalized data values to digital values.

The Lin patent is a digital filter that operates on digital sample values of data (specifically voice), whereas Lin's implementation can not execute analog samples as it is using flipflops to delay data samples, which is not possible for analog samples.

Moreover, Lin's FIR filter does not use multiple phases of clock to generate the "analog" data samples that are spaced in time with a certain time difference that is determined by the phase spacing of the clock. In Lin's implementation the delayed version of the "digital" is achieved by a very basic flipflop pipeline.

Additionally, the output of the proposed filter runs at symbol rate and thus requires the whole circuitry to run at symbol rate which is acceptable for voice frequency range of several kHz or even several MHz, while one of the main advantages of the current patent application is the fact that the sampling clock has multiple phases running at a divided down version of the data frequency and thus the circuit is capable of processing input data at well beyond multiple GHz range.

Khoury's patent directly addresses the FIR operation on analog sampled data and the fact that the analog data samples are spaced in time using a multi-phase sampling clock. However, the main differentiation of the present invention is that the proposed FIR filter runs at a fraction of the input data frequency (determined by the frequency of the sampling clock that is a divided version of the input data frequency), while in Khoury's patent the FIR filter runs exactly at the

input data frequency. This characteristic of Koury's invention puts a significant speed requirement on the FIR circuit and makes it completely impractical for multi-GHz applications.

Another disadvantage of Khoury's patent is that it needs to rotate the tap coefficients applied to data samples at input data frequency. Tap coefficients accuracy directly define the accuracy of the FIR filtering. Therefore, if the tap coefficients do not have enough time to settle within the bit time, the filtering process will be inaccurate. This is a serious problem at very high speeds in that bit time is very small (e.g., less than 1nsec at frequencies above 1Gbps), and therefore makes it impractical to implement Khoury's proposed topology at multi-Gbps rates.

A final disadvantage of Khoury's architecture is sensitivity to mismatch between the tap weight scaler circuits. When data samples are modulated at different scaler stages with ideally the same coefficient (same coefficient is rotated around), they will be scaled by a different value due to the mismatch of the scalers. In the present invention such a problem does not exist, because tap weights are fixed to each scaler, and scaler mismatch does not affect filter accuracy, as long as each scaler coefficient is adjusted independently.

Accordingly, for the above-identified reasons, independent claims 1, 11 and 15 are allowable over the cited references. Furthermore claims 2-10 and and 12-14 are allowable since they depend from allowable base claims.

Claims 16-18

Independent claims 16-18 are reproduced in their entirety hereinbelow.

16. A multi-tap analog finite impulse response filter, comprising:
at least one combined voltage-current converter and scaler that produces a first current from an input voltage which is proportional to a product of a previous data sample voltage and a weight associated with said previous data sample tap;
a voltage-current converter that produces a second current which is proportional to an instance data sample voltage;
an adder circuit which subtracts the second current from the first current to produce a

third current; and

a converter circuit which converts the third current to a voltage corresponding to the equalized data voltage.

17. A multi-tap analog finite impulse response filter method, comprising:

producing at least a first current from an input voltage which is proportional to a product of a previous data sample voltage and a weight associated with said previous data sample tap;

producing a second current which is proportional to an instance data sample voltage;

subtracting the second current from the first current to produce a third current; and

converting the third current to a voltage corresponding to the filtered data bit.

18. A multi-tap analog finite impulse response filter, comprising:

means for producing at least a first current from an input voltage which is proportional to a product of a previous data sample voltage and a weight associated with said previous data sample tap;

means for producing a second current which is proportional to an instance data sample voltage;

means for subtracting the second current from the first current to produce a third current; and

means for converting the third current to a voltage corresponding to the filtered data bit.

As before mentioned, the Lin patent is a digital filter that works on digital sample values of data (specifically voice), whereas Lin's implementation can not execute analog samples as it is using flipflops to delay data samples, which is not possible for analog samples.

Moreover, Lin's FIR filter does not use multiple phases of clock to generate the "analog" data samples that are spaced in time with a certain time difference that is determined by the phase spacing of the clock. In Lin's implementation the delayed version of the "digital" is achieved by a very basic flipflop pipeline.

Khoury's patent utilizes current based sampling, and thus the input signal has to be in the form of current. This is a limitation for the design as almost all ICs accept voltage rather than current. As is recited in independent claims 16-18, the input signal of the present invention comprises an input voltage which is converted by the combined voltage converter and scaler.

Khoury uses a feedback amplifier cell to track and hold the input current value. Feedback

amplifiers tend to burn much more current than open loop amplifiers, or thus burn much slower for the same power level. The present invention uses an open-loop circuit as recited in new claim 20 for the combined voltage-current converter and scaler.

Khoury performs tap weight scaling by using a complex resistor network. The present invention accomplishes tap weight scaling by modulating the source current or effectively the relative strength of the voltage-current converters as recited in claims 19 and 20.

Applicant submits therefore that independent claims 16-18 are allowable over the cited references. In addition, claims 19-21 dependent thereon are allowable since they depend from an allowable base claim.

In view of the foregoing, it is submitted that the claims 1-21 are allowable over the cited references and are in condition for allowance. Applicant respectfully requests reconsideration of the rejections and objections to the claims, as now presented.

Applicants' attorney believes this application in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted,
SAWYER LAW GROUP LLP

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